Reg.No. \_\_\_\_\_\_\_\_\_\_\_\_



**UNIVERSITY**

(Karunya Institute of Technology & Sciences)

(Declared as Deemed-to-be University under Sec.3 of the UGC Act, 1956)

**End Semester Examination – Nov/Dec – 2016**

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|  |  | **Semester :** | **2016-17 ODD** |
| **Code :** | **14EC2068** | **Duration :** | **3hrs** |
| **Sub. Name :** | **VHDL** | **Max. marks :** | **100** |

**ANSWER ALL QUESTIONS (5 x 20 = 100 Marks)**

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| **Q. No.** | **Sub Div.** | **Questions** | **Course**  **Outcome** | **Marks** |
| 1. | a. | Explain different classes of data objects in detail with example. | CO1 | 10 |
| b. | What are the different data types in VHDL? Explain briefly scalar data type. | CO1 | 10 |
| (OR) | | | | |
| 2. | a. | Explain briefly about the various Data operators used in VHDL based system design? | CO1 | 10 |
| b. | Describe the general roles of the following VHDL constructs i. Entity declaration ii. Architecture body | CO1 | ( 5 + 5) |
| 3. | a. | Write VHDL code for full adder. | CO2 | 6 |
|  | b. | Write the VHDL program for 4:1 MUX using conditional and the selected signal assignment statement. | CO2 | 14 |
| (OR) | | | | |
| 4. | a. | Explain briefly about the various concurrent signal assignment statements? | CO2 | 10 |
|  | b. | Design a 4-bit Binary counter using Process statement. | CO2 | 10 |
| 5. | a. | Using Data flow modeling design a Full subtractor logic? | CO2 | 10 |
|  | b. | Design a 2 bit magnitude comparator in Behavioral modeling using VHDL. | CO2 | 10 |
| (OR) | | | | |
| 6. | a. | Write a program for a 4 bit adder using structural modeling in VHDL. | CO2 | 10 |
|  | b. | Explain in detail the Positional and Named association in Component Instantiation. | CO2 | 10 |
| 7. | a. | Give the basic structure of a test bench in VHDL. | CO3 | 8 |
|  | b. | Write an VHDL code for a Traffic light controller. | CO3 | 12 |
| (OR) | | | | |
| 8. | a. | Write the differences between VHDL functions and procedures. | CO3 | 10 |
|  | b. | Discuss the package declaration and package body with an example. | CO3 | 10 |
|  | | **Compulsory:** |  |  |
| 9. | a. | Write short notes on:  a.Operator overloading b. Libraries | CO3 | (5 + 5) |
|  | b. | Compare inertial delay and transport delay in VHDL. | CO3 | 10 |

ALL THE BEST